European Journal of Engineering Science and Technology
ISSN 2538-9181

Design and Experimental Verification of a Single-Phase Asymmetric Hybrid Multi-Level Inverter

Mustafa Deniz, Ali Osman Arslan, and Ahmet Mete Vural*

Electrical and Electronics Engineering Department, Gaziantep University, Gaziantep, Turkey

ARTICLE INFO

Keywords:
Multi-level inverter
Asymmetric operation
Hybrid topology
Phase disposition pulse width modulation
Experimental verification

ABSTRACT

In recent years, multi-level inverters have emerged as a feasible power conversion solution for medium and high-power applications due to better harmonic performance and ability to operate at high voltage/power when compared to traditional two-level inverters. Since the output level of the multi-level inverters depends on the number of the switching elements, as more levels are required, more switching elements are used. This situation makes the circuit and the control design complex and the losses to upsurge. To overcome these limitations and produce low harmonic content at the output, reduced switch count topologies are popular. In this study, a single-phase asymmetric hybrid multi-level inverter is proposed by combining diode clamped and cascaded H-bridge topologies. The inputs of the proposed inverter are selected as two unequal DC voltage sources. In this regard, fewer switching elements are used to obtain the same number of voltage levels at the output when compared to traditional multi-level inverters. The efficiency and the harmonic performance of the proposed topology is both verified by simulation and experimental studies. The gating signals of the semiconductor switches are produced by phase disposition pulse width modulation with carriers' frequency of 4 kHz. It is shown by the experiments that a maximum efficiency of 94 % and a total harmonic distortion of 29 % are attained in the case studies.

1. Introduction

Inverters are the key element in DC to AC power conversion with a variety of voltage/power levels in either single-phase or three-phase electrical systems. In recent years, inversion technology has evolved promptly so that the inverters have a wide range of application area, such that industrial applications (El-Zohri et al., 2019), power supplies (Buccella et al., 2019), electrical vehicles (Li et al., 2019), renewable energy systems (Zeb et al., 2018), microgrids (Sahoo et al., 2020), HVDC transmission systems (Barnes et al., 2017), and more. The basic inverter type is the two-level one in which two/six semiconductor switches for single/three-phase operation are controlled to generate an AC voltage with desired magnitude and frequency at the output from a fixed DC input (Mali et al., 2019). Although two-level inverters are easy to construct with low number of semiconductor switches, large filter size and high switching frequency problems limit their utilization especially for medium/high power applications. In this sense, especially, multi-level inverter (MLI) topology readily becomes an alternative approach with modularity, reduced voltage/current stress on semiconductors, reduced harmonic distortion/electromagnetic interference, and transformerless operation in medium/high power applications (Vijeh et al., 2019). MLIs are conventionally divided into three main types in terms of circuit topology: neutral point or diode clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB). NPC and FC MLIs are easy to implement for

* Corresponding Author E-Mail Address: mvural@gantep.edu.tr

low voltage levels such as five or less. But, for higher levels, they become impractical due to capacitor voltage balancing issue (Shults et al., 2018), (Giri et al., 2019). CHB MLIs operate with isolated multi-DC links and get more attention in spreaded grid-connected applications (Zheng et al., 2013), (Hasan et al., 2017), (Cornize et al., 2002), (Chen et al., 2016), especially renewable energy systems (Islam et al., 2013), (Karasani et al., 2017), (Rivera et al., 2011). Regardless of the topology, inverters are mainly composed of a DC input, power semiconductor switches, isolation, driver, and control circuits as well as filters. In this regard, many studies have been carried out to improve the inverter operation in terms of efficiency, harmonic content, and DC voltage utilization. These research efforts are usually conducted on developing novel circuit topologies, control methods, modulation strategies, filter design, and more (Peng et al., 2010) (Akagi et al., 2019) (Montesinos-Miracle et al., 2013) (Holmes et al., 2001). In principle, hybrid inverters can be designed by combining the aforementioned MLI topologies to get higher efficiency and lower harmonic content when compared to traditional MLI topologies. In a hybrid MLI, each module can be constructed from a different MLI circuit which can operate at different voltage levels and switching frequencies (Abraham et al., 2014). For instance, a multi-level hybrid MLI topology consisting of NPC and FC MLIs is proposed for high power induction motor drives (Viju et al., 2018). A seventeen-level hybrid MLI constructed from the combination of FC and CHB MLIs together with floating capacitors is suggested in (Kumar et al., 2015). A hybrid MLI topology from the mixture of NPC and CHB MLIs is presented for a transformerless grid connected photovoltaic power plant (Chattopadhyay et al., 2012). MLIs are called symmetric if they are operated with an equal DC voltage source in each module. Alternatively, MLIs are called asymmetric if an unequal DC voltage source for each module is utilized. The benefit of the asymmetric operation is that more voltage levels hence low harmonic content at the output is obtained for the same number of semiconductors when compared to symmetrical MLI topologies. In this study, a single-phase seven-level asymmetric hybrid MLI topology is proposed by combining NPC and HB MLI topologies. The design is made in the simulation platform and the experiemental verification of the hardware setup of the proposed MLI is carried out for different power factor loads under changing modulation indices. It is experimentally shown that the proposed MLI has a maxium efficiency of 94 % and generates a total harmonic distortion of around 29 %. The organization of the paper is as follows: After the introductory section, Section 2 introduces the power stage of the proposed MLI. The implementation of the modulation scheme in the simulation platform is mentioned in Section 3. The simulation studies including harmonic and efficiency measurements are presented in Section 4. The hardware setup of the proposed MLI is introduced in Section 5. The efficiency and harmonic measurements taken from the experimental setup are also provided in this section. Finally, the conclusion is drawn in Section 6.

2. Power Circuit of the Proposed MLI

The simulation model of the proposed MLI including the power circuit is represented in Figure 1. This simulation model is needed prior to experimental study in order to verify the modulation scheme for the semiconductor switches and choose the ratings of the components. Moreover the proposed MLI can be tested in this design stage in terms of efficiency and harmonic content. The design consists of an NPC module and an HB module connected in cascaded manner. The NPC module consists of four MOSFETs, two diodes, and two DC sources (12 V for each). The HB module consists of four MOSFETS and one DC source (24 V). The choice of different DC sources (24 V/12 V=2) is a result of asymmetrical operation in which maximum seven-levels can be obtained at the output voltage. It is important to mention that only five-levels can be obtained at the output if equal DC sources were used in the symmetrical operation. These DC sources are chosen such that they can be found easily in daily life. The MOSFET is chosen as the switching element instead of IGBT, since MOSFETs are more advantageous in inverter

applications with rating of 500 W or less and 250 V rms or less (Rashid, 2001). Two different loads are considered both in simulation and experimental studies. The first load is the unity power factor load with R=10 Ω. The power factor of the second load is 0.9 lagging with R=10 Ω and L=15 mH. The pulse generation block for the MOSFETs are also shown in Figure 1. This block computes the switching instant of each MOSFET according to the phase disposition pulse width modulation (PDPWM) technique, discussed in the next section.

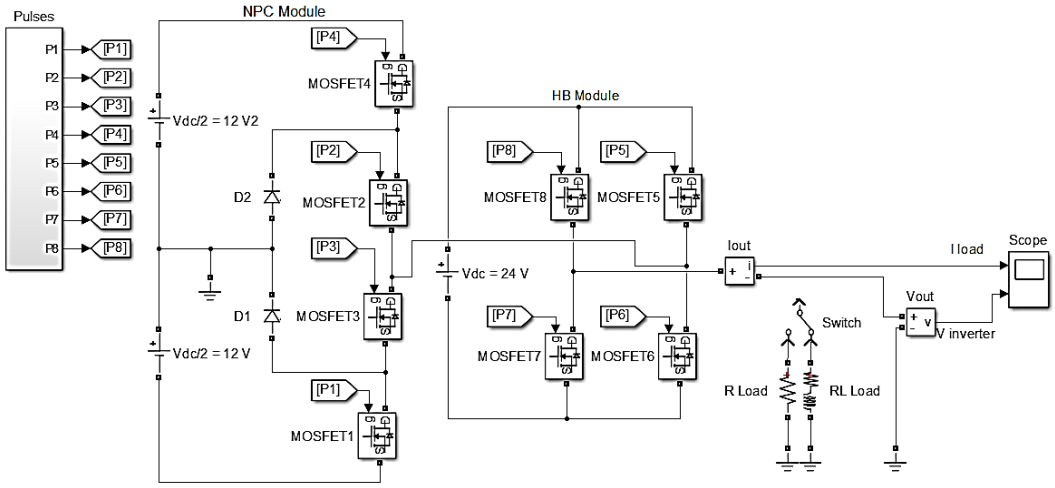


Figure 1.
The Simulation Model of the Proposed MLI

3. Phase Disposition Pulse Width Modulation

Phase disposition pulse width modulation (PDPWM) technique is an extension of classical sinusoidal PWM to MLIs. In classical sinusoidal PWM, a sinusoidal reference signal is compared to a sawtooth/triangle carrier signal usually with a frequency of 1 kHz or more. In fact, there are two main modulation techniques for MLIs which have many carriers depending on the number of modules being used: phase shifted PWM and level shifted PWM. Generally, these carriers have same frequency and amplitude. In phase shifted PWM, the carriers are phase shifted while the positions of positive/negative peaks are same. But, in case of level shifted PWM, only the positions of positive/negative peaks are altered in accordance with the module number while the phase angles of the carriers are kept equal. PDPWM is the sub category of the level shifted PWM technique in which *N-1* carriers are used to generate *N*-level voltage at the output (Arslan et al., 2019). The simulation model of the PDPWM technique used in this work is shown in Figure 2. As shown, six sawtooth carrier signals are compared with a reference sinusoidal signal using comparators. In all simulation as well as experimental studies, the frequency of the reference signal and that of each carrier is chosen as 50 Hz and 4 kHz, respectively. Figure 3 shows the generated gating signals (P1-P8) for the MOSFETs by using PDPWM technique for a modulation index of $m_a = 1$. Note that P1, P3, P5, and P7 are the complements of P2, P4, P6, and P8, respectively. This is necessary since one MOSFET is turned on, the complement of this MOSFET must be turned off to prevent a possible short circuit in the DC source. In asymmetrical operation, the output voltage of the proposed MLI switches between +/-36 V with maximum seven different levels as shown in Table 1. Each voltage level at the output is obtained by an appropriate switching combination. For example, to see 36 V at the output, MOSFETs with numbers 2,4,6,8 should be turned on, while MOSFETs with numbers 1,3,5,7 should be turned off.

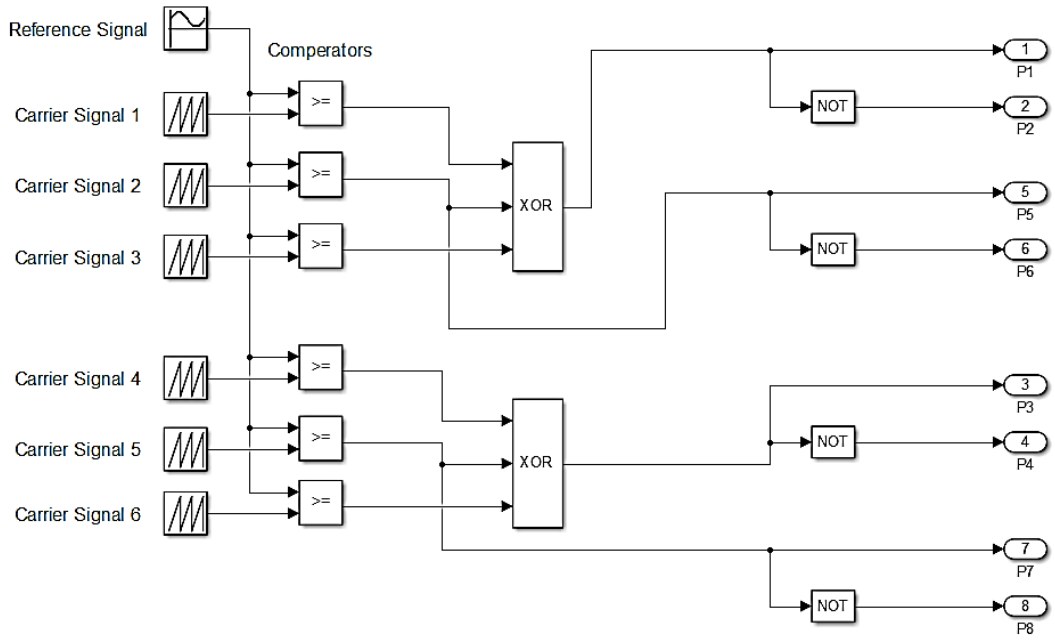


Figure 2.
The Simulation Model of the PDPWM Technique

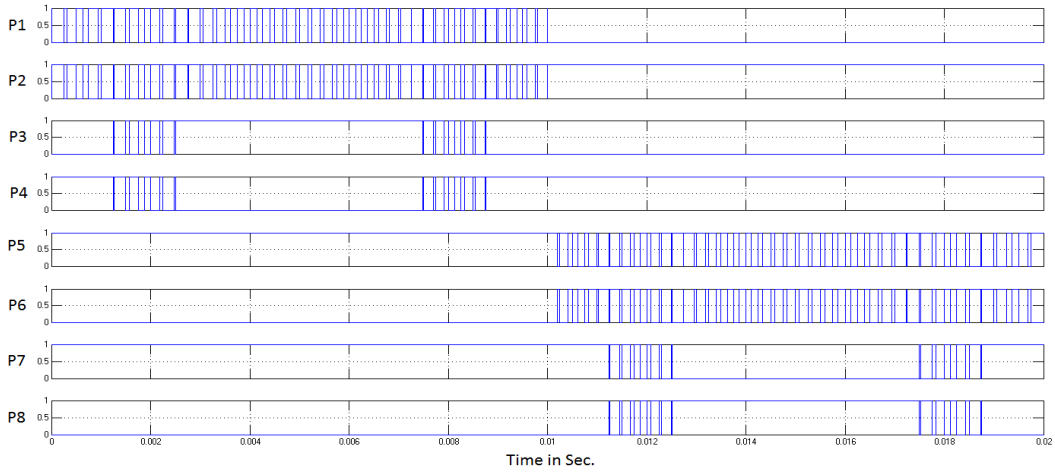


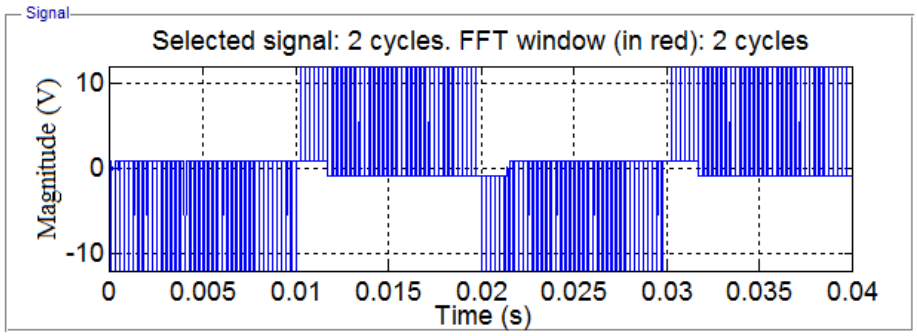
Figure 3.
The Gating Signals of the PDPWM Technique for a Modulation Index of $m_a = 1$

Table 1.
Switching States of the Proposed MLI

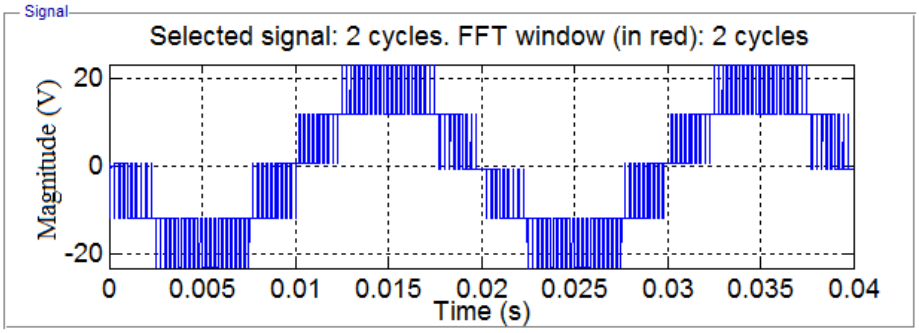
Level	P1	P2	P3	P4	P5	P6	P7	P8
-36 V	1	0	1	0	1	0	1	0
-24 V	0	1	1	0	1	0	1	0
-12 V	1	0	1	0	1	0	0	1
0 V	0	1	1	0	1	0	0	1
12 V	0	1	0	1	1	0	0	1
24 V	0	1	1	0	0	1	0	1
36 V	0	1	0	1	0	1	0	1

4. Simulation Studies

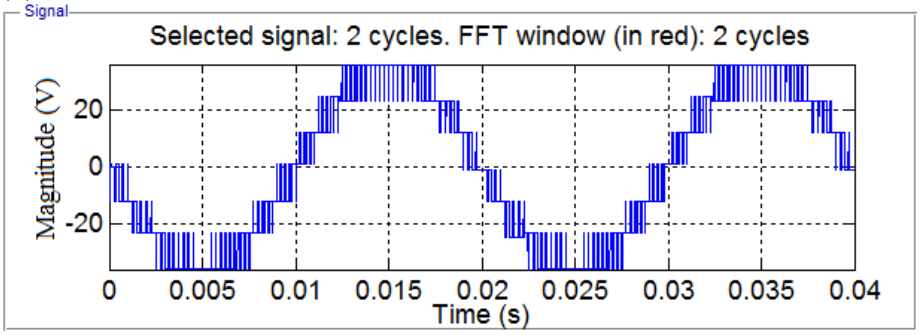
The simulation model of the proposed MLI is executed to verify the output voltage waveform. Figure 4 shows the open-circuit output voltage waveforms of the proposed MLI at different modulation indices. As shown, a symmetrical voltage waveform at each modulation index is attained with a period of 20 ms. Also, it is observed that as the modulation index is increased, the voltage levels increase as well. More specifically, Figure 4 (a) shows that the level number is three when m_a is set to 0.1. As m_a is increased, for instance, at $m_a = 0.5$ and $m_a = 1.0$, the number of output voltage levels is five and seven, respectively, observed in Figure 4 (b) and (c), respectively.



(a)



(b)



(c)

Figure 4.
Output Voltage Waveforms of the Proposed MLI at Different Modulation Indices, (a) $m_a = 0.1$, *(b)* $m_a = 0.5$, *(c)* $m_a = 1.0$

4.1. Harmonic Analysis

Power electronic systems are non-linear so that they generate non-sinusoidal voltage and current waveforms. In this regard, MLIs produce distorted voltage/current waveforms at their output including varying amount of harmonics which cause problems such as losses, device malfunctions, interferences in communication systems, and etc (Ma et al., 2018). Total harmonic distortion (THD) is a measure of the power quality in electrical power systems, which

determines the quantity of the harmonics available in a voltage/current waveform. THD is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. By increasing the level number at the output voltage in a MLI, the voltage waveform much resembles a pure sinusoid. Hence, one way to reduce THD is to design MLIs having many voltage levels at the output. Other factors are also effective on the power quality of the MLIs, such as the modulation type for semiconductor switching and the magnitude of modulation index. In practice, the number of voltage levels at the output of the MLIs cannot be increased so easily, due to control difficulty, increasing losses, and capacitor voltage balancing problem. In this regard, this study aims to design an asymmetrical MLI that generates more voltage levels to reduce THD at the output when compared to a symmetrical MLI having the same number of semiconductors. In simulations, the frequency of the reference sinusoidal waveform and that of the carriers are chosen as 50 Hz and 4 kHz, respectively. At first, the power quality of the proposed MLI is investigated in terms of THD as the modulation index is varied. The results are presented in Figures 5 and 6, for unity and lagging power factor load, respectively. Figure 5 shows the change of THD of output voltage waveform with respect to modulation index when a resistive load of R=10 Ω is connected at the output of the proposed MLI. As seen, the highest THD is recorded when m_a is minimum. As the modulation index is increased, the THD drops sharply due to the fact that the number of voltage levels at the output increases. With this respect, the smallest THD is less than 25 % when $m_a = 1.0$. Figure 6 shows the change of THD of output voltage waveform with respect to modulation index when a lagging load (R=10 Ω, L=15 mH) is connected at the output of the proposed MLI. As seen, the highest THD is recorded when m_a is minimum. As the modulation index increases, the THD drops as in case of resistive load due to the fact that the number of voltage levels at the output increases as m_a increases. With this regard, the minimum THD is obtained less than 25 % when $m_a = 1.0$.

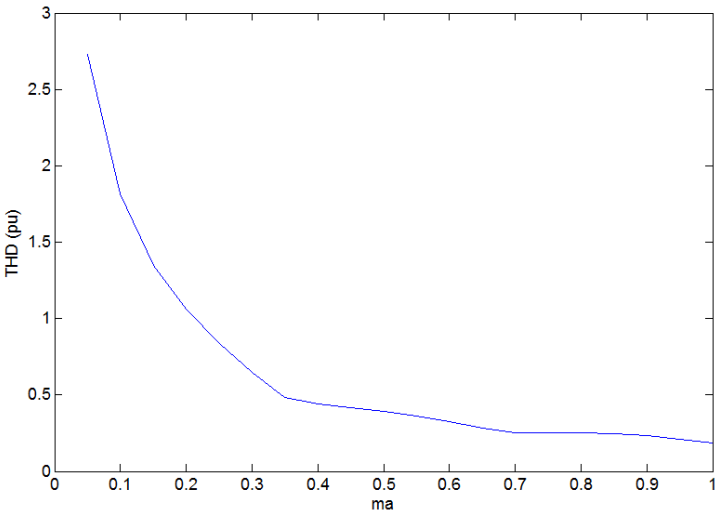


Figure 5.
THD of Voltage of a Resistive Load (R=10 Ω) Connected at the Output of the Proposed MLI

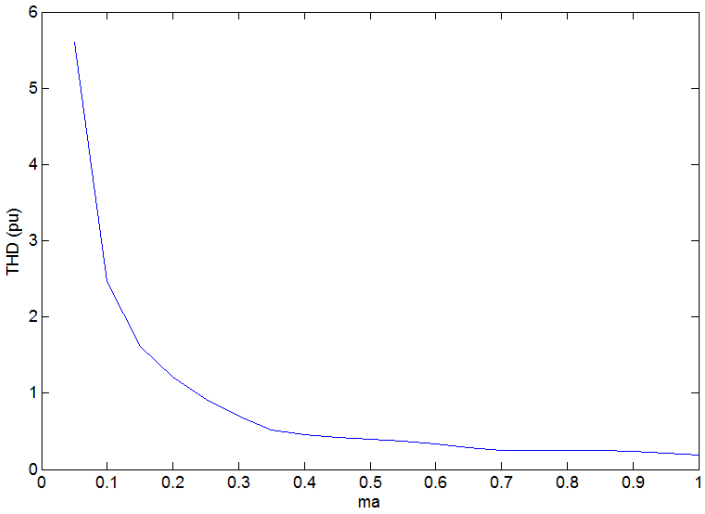
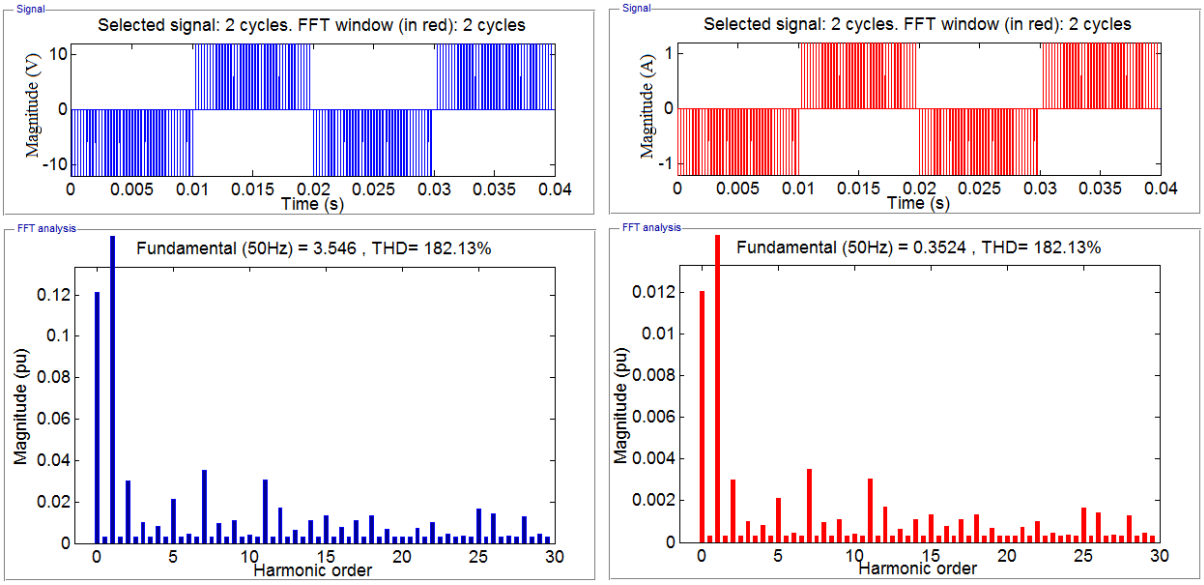


Figure 6.
THD of Voltage of a Lagging Load (R=10 Ω, L=15 mH) Connected at the Output of the Proposed MLI

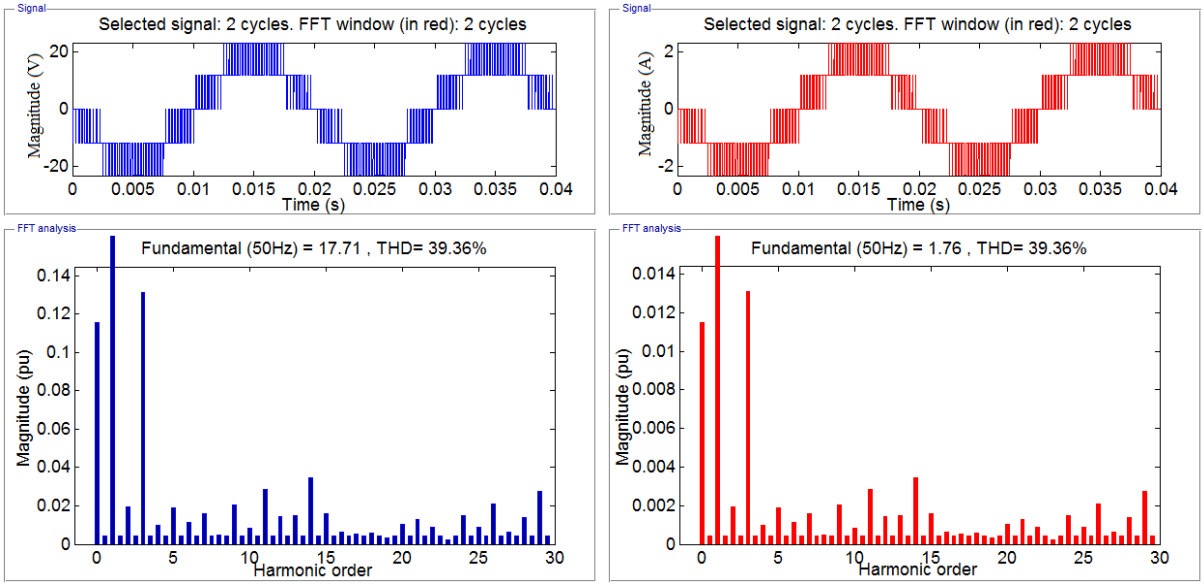
To observe the individual harmonics present in the load voltage/current waveforms of the proposed MLI, a Fast Fourier Transform (FFT) analysis is conducted as a second study to convert the simulated waveforms into the frequency domain. In the FFT analysis, fundamental frequency is 50 Hz and the maximum harmonic number that will be investigated is chosen as 30. The FFT analysis results for both resistive and lagging loads of the proposed MLI under different modulation indices are illustrated in Figures 7-12. It is observed in all figures that the even harmonics are minimum or do not exist due to the symmetrical waveform generation of the proposed MLI. Moreover the most dominant harmonic is the third one followed by fifth and seventh harmonics. In Figure 7, the level number at the output voltage/current waveform of the proposed MLI is three when $m_a = 0.1$. Accordingly the THD is very high and the most strong harmonics are observed in this case. As seen in Figures 8 and 9, the output voltage and current waveforms approach to a perfect sinusoidal waveform after increasing the modulation index. In this regard, the THD of output voltage/current of the proposed MLI for resistive load is 39.36 % for $m_a = 0.5$ and 18.68 % for $m_a = 1.0$, respectively. On the other hand, Figures 10-12 show that the THD of output voltage for lagging load reduces down to 18.81 % after increasing the modulation index up to $m_a = 1.0$. The THD of output current for lagging load is quite low when compared to output voltage, as observed in Figures 10-12. The current THD decreases down to around 6 % after increasing the modulation index up to $m_a = 1.0$.



(a) (b)

Figure 7.

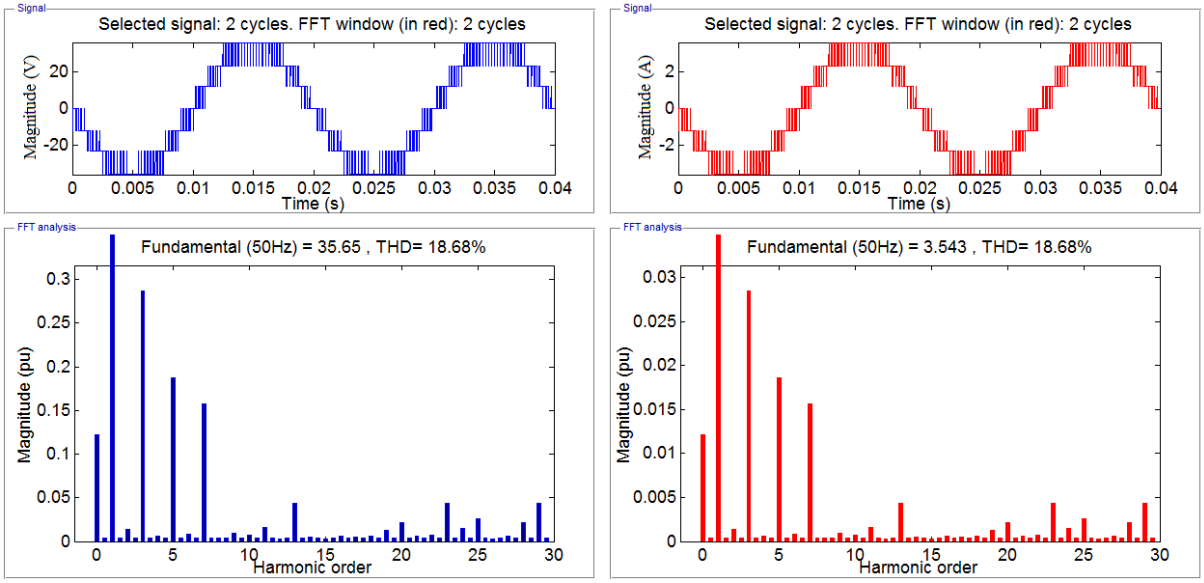
Harmonic Spectrum of (a) Vand (b) Current of Resistive Load (R = 10 Ω) at $m_a = 0.1$



(a) (b)

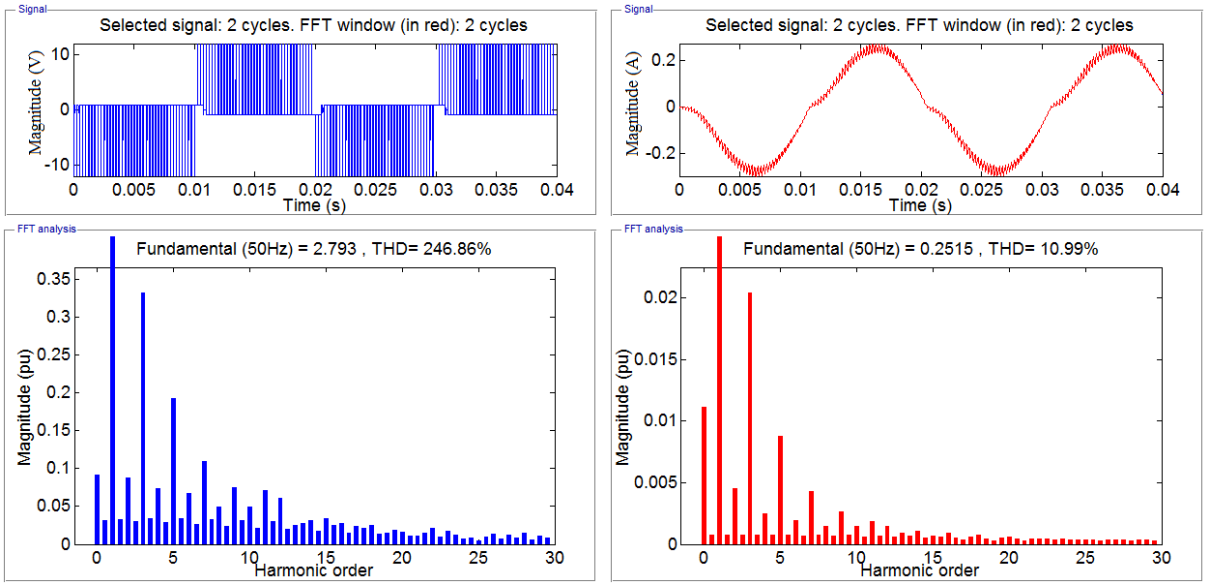
Figure 8.

Harmonic Spectrum of (a) Voltage and (b) Current of Resistive Load (R = 10 Ω) at $m_a = 0.5$



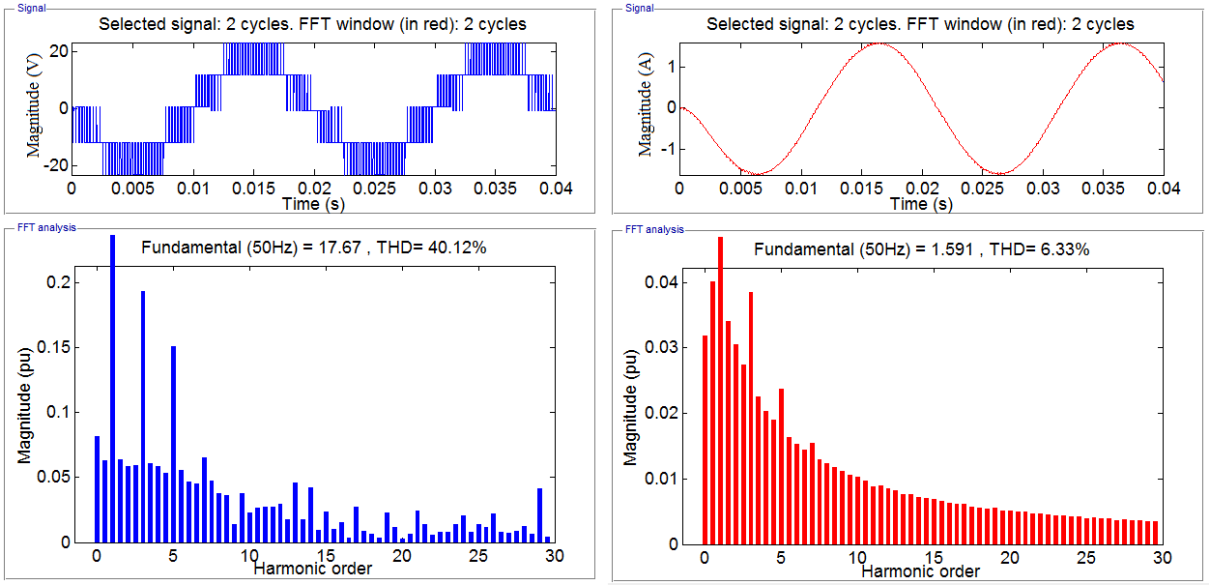
(a) (b)

Figure 9.
Harmonic Spectrum of (a) Voltage and (b) Current of Resistive Load (R = 10 Ω) at $m_a = 1.0$



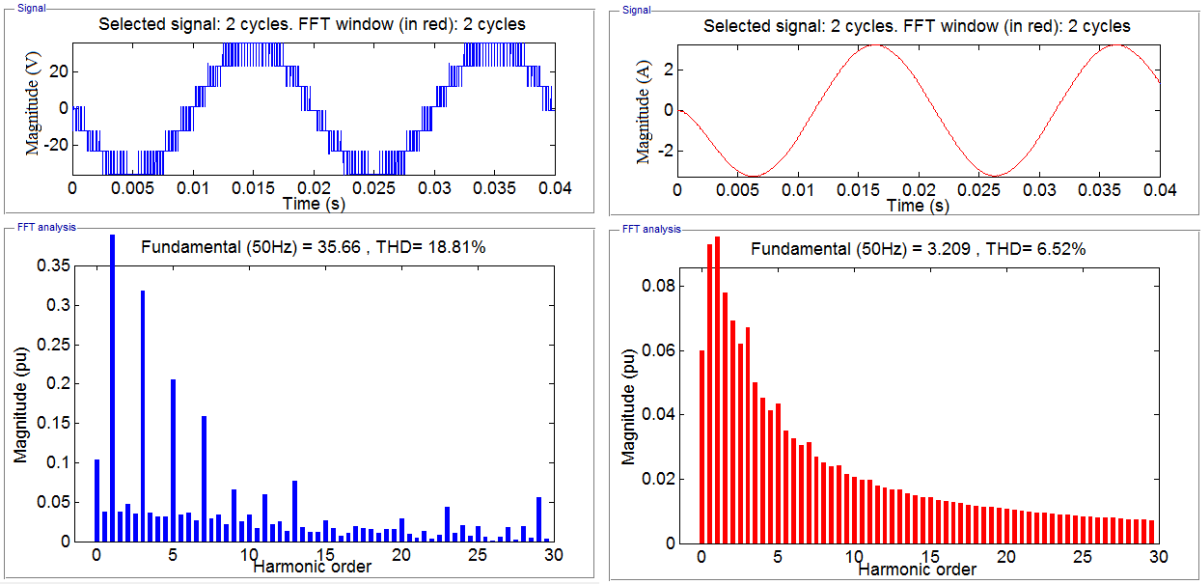
(a) (b)

Figure 10.
Harmonic Spectrum of (a) Voltage and (b) Current of Lagging Load (R=10 Ω, L=15 mH) at $m_a = 0.1$



(a) (b)

Figure 11.
Harmonic Spectrum of (a) Voltage and (b) Current of Lagging Load (R=10 Ω, L=15 mH) at $m_a = 0.5$



(a) (b)

Figure 12.
Harmonic Spectrum of (a) Voltage and (b) Current of Lagging Load (R=10 Ω, L=15 mH) at $m_a = 1.0$

4.2. Efficiency Analysis

In this section, the efficieny of the proposed MLI when feeding different power factor loads under different modulation indices is investigated. In the simulations, the frequency of the reference sinusoidal waveform and that of the carriers are chosen as 50 Hz and 4 kHz, respectively. The efficiency of the MLI can be calculated as the percentage ratio of the output active (real) power of the MLI to the total input DC power of the MLI. The input power of the proposed MLI is found by summing up all three input power of each DC voltage source connected to the NPC and HB modules. The input power of each DC voltage source is calculated by multipliying the DC voltage with the mean value of the current of the DC voltage source. On the other hand, the output active power of the MLI when a load is connected is calculated by the production of rms load voltage, rms load current, and the power factor of the

load. Accordingly, the efficiency of the proposed MLI at unity (R=10 Ω) and lagging power factor (R = 10 Ω, L = 15 mH) loads are listed in Table 2 and 3, repectively when different modulation indices are chosen. Reference to Table 2, the efficiency of the MLI increases continuously from 23.08 % to 95.73 % for resistive load when m_a is increased from 0.1 to 1.0. Table 3 shows that the efficiency of the MLI continuously increases for lagging load when m_a is increased from 0.1 to 1.0. For both load types, when the modulation index is set to maximum ($m_a = 1$), the highest efficiency of the proposed MLI (95.73 % for resistive load and 98.81 % for lagging load) is obtained.

Table 2.
The Efficiency of the Proposed MLI for Resistive Load (R=10 Ω)

m_a	Input power	Output power	Efficiency
0.1	2.71 W	0.62 W	23.08 %
0.2	5.47 W	2.57 W	46.91 %
0.3	8.19 W	5.75 W	70.26 %
0.4	12.28 W	10.19 W	82.98 %
0.5	18.35 W	15.59 W	84.96 %
0.6	25.16 W	22.14 W	88.00 %
0.7	32.69 W	29.90 W	91.47 %
0.8	42.77	39.41	92.14 %
0.9	54.04	50.52	93.49 %
1.0	65.99	63.17	95.73 %

Table 3.
The Efficiency of the Proposed MLI for Lagging Load (R = 10 Ω, L = 15 mH)

m_a	Input power	Output power	Efficiency
0.1	0.43 W	0.32 W	73.39 %
0.2	2.02 W	1.83 W	90.60 %
0.3	4.69 W	4.51 W	96.08 %
0.4	8.45 W	8.26 W	97.74 %
0.5	13.34 W	13.03 W	97.68 %
0.6	19.10 W	18.57 W	97.22 %
0.7	25.90 W	25.11 W	96.95 %
0.8	33.98 W	33.12 W	97.45%
0.9	43.26 W	42.46 W	98.15 %
1.0	53.75 W	53.11 W	98.81 %

5. Experimental Study

The experimental prototype of the proposed single-phase asymmetric hybrid MLI is shown in Figure 13. The power circuit of the proposed MLI consists of NPC module, HB module, microcontroller/measuring circuit on the same card. An isolated power supply is also needed for the microcontroller and the measuring circuit. Figure 13 also shows separate DC sources for each module, load, and the measurement devices in the laboratory. PIC18F4431 type microcontroller is used to generate the gating pulses of the MOSFETs because of its simple programming capability and processing speed. Eight IXTP230N075 MOSFETs which have a current and voltage rating of 230 A and 75 V are used in the design. FOD3182 optocouplers and IRS2110 gate drivers are used for isolation and driving the MOSFETs, respectively. Two

12 V and one 24 V DC sources are used at the input side of the proposed MLI. To get 24 V, two 12 V/7 Ah batteries are connected in series. These batteries are able to supply continuous and stable power to the proposed MLI. Designing the dead-time is crucial in the inverter design. It is theoretically assumed that all MOSFETs are turned on and off at the desired time in the simulations. But this is not possible in practice due to the switching characteristics of the real power semiconductors. For instance a switch can be turned on before the other switch is turned off on the same leg. This situation causes a short circuit for DC sources which can greatly damage the batteries. Thus, an appropriate dead-time must be considered and embedded in the modulation algorithm of the switches in voltage source inverters. Improper choice of the dead-time can lead to voltage reduction and the current distortion at the inverter output (Xiaofang et al., 2011), (Narmatha et al., 2013). In this study, 3.3 µs dead-time is added to the PDPWM algorithm in the microcontroller to prevent any short ciruit in the MLI circuit. In the experimental studies, the output voltage and current waveforms of the proposed MLI are captured by 200 MHz Tetronix TPS 2024 type oscilloscope.

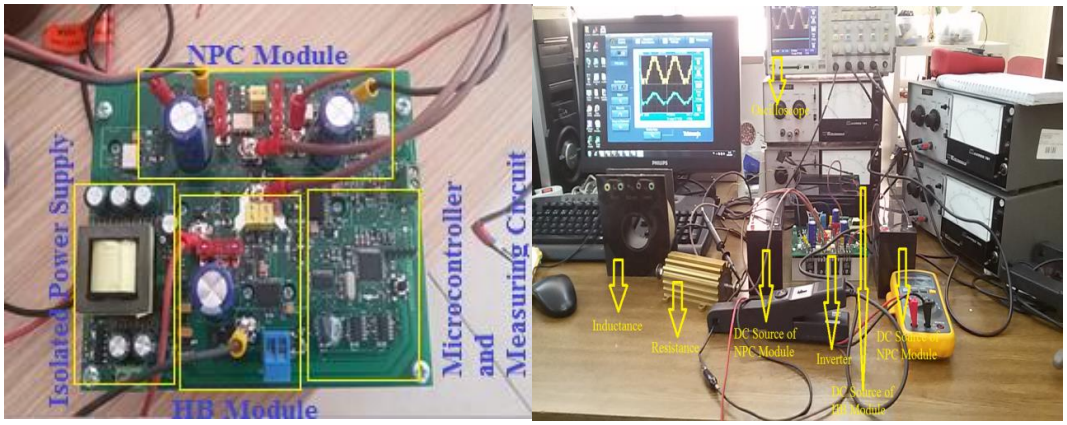


Figure 13.
Experimental Prototype of the Proposed MLI

5.1. Harmonic Analysis

The harmonic performance of the proposed MLI is investigated experimentally in this section. Figure 14 shows the voltage and current waveforms of the proposed MLI when a resistive load (R=10 Ω) is connected at the output. Figure 15 shows the voltage and current waveforms of the proposed MLI when a lagging load (R=10 Ω, L=15mH) is connected at the output. For both loading cases, the modulation index is chosen as $m_a = 1.0$ and the frequency of the PDPWM carriers is programmed as 4 kHz in the microcontroller. It is observed that the experimental measurements are consistent with the simulation results in terms of waveform shape. The level number of the output voltage is seven and the magnitude of each level is comparable with the simulation results. In the experimental studies, the measurement data are taken from the oscilloscope in csv format and transferred to the simulation program to evaluate FFT analysis. The harmonic analysis of the output voltages for both load types are presented in Figures 16 and 17, repectively for resistive and lagging loads. It is observed that the THD analysis of the experimental results does not perfectly fit with the simulation results under the same operating conditions of the proposed MLI. In detail, at the modulation index of $m_a = 1.0$, the THD of the output voltage of the resistive/lagging load is calculated as 18.68 % and 18.81 %, respectively in the simulation studies. On the other hand, the THD of the output voltage of the resistive/lagging load is both calculated as 29.46 % during the experiments. The increase in THD measurements during the experiments is due to the nonidealities of the components, snubber circuits, and the small measurement errors which are not fully considered in the

simulation studies. Although no filter is proposed in this study, the THD of the voltage/current at the output of the proposed MLI can be further decreased practically with a filter connected before the load.

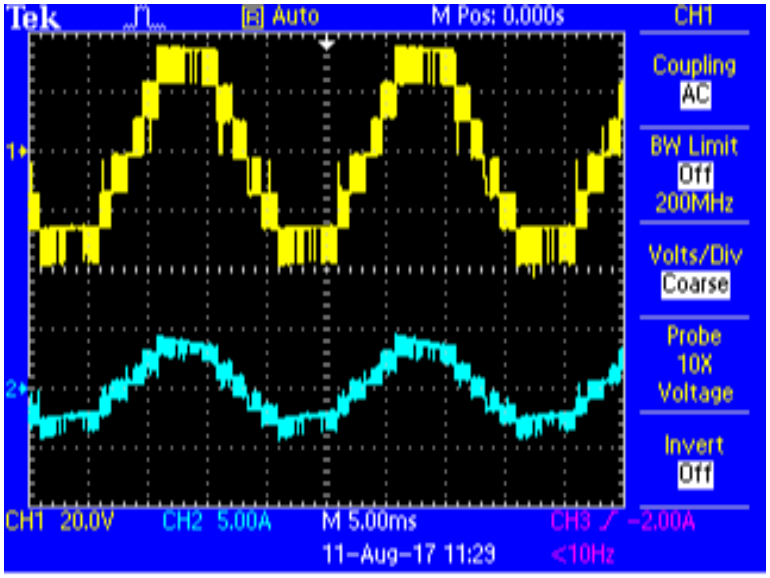


Figure 14.
Output Voltage and Current of the Resistive Load (R = 10 Ω) at $m_a = 1.0$

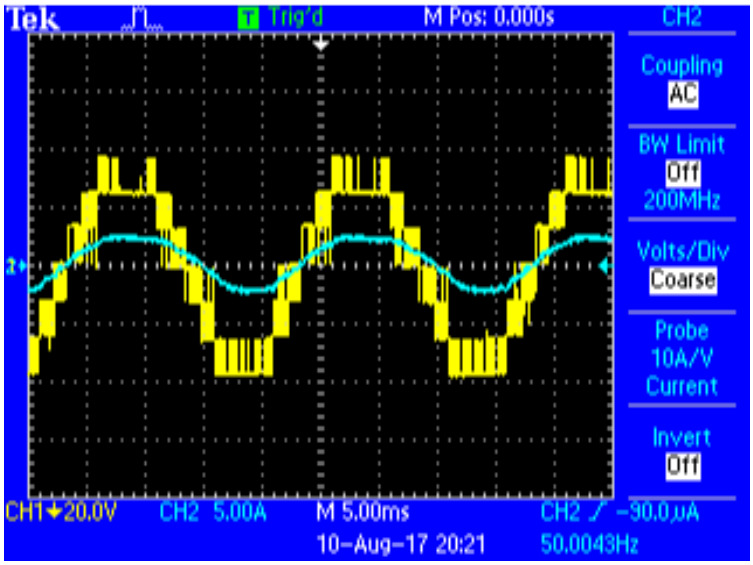


Figure 15.
Output Voltage and Current of Lagging Load (R = 10 Ω, L = 15mH) at $m_a = 1.0$

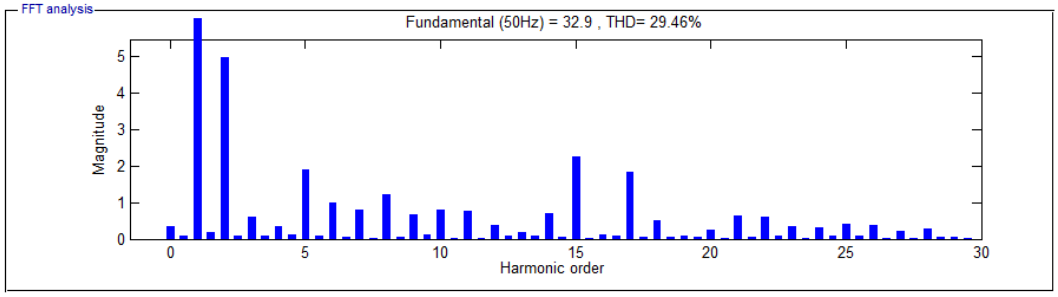


Figure 16.
Harmonic Spectrum of Output Voltage of the Resistive Load (R = 10 Ω) at $m_a = 1.0$

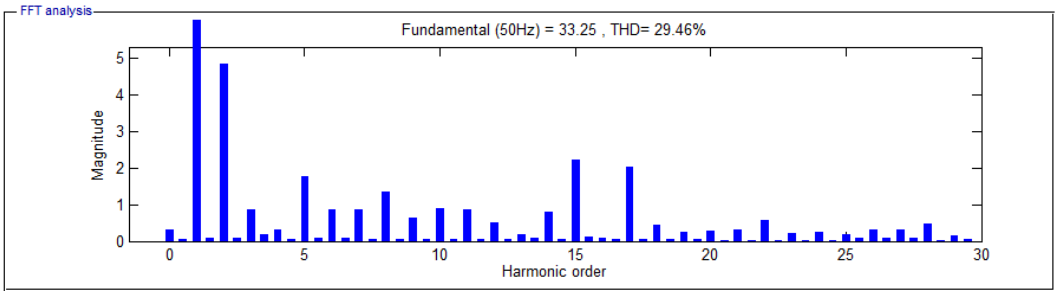


Figure 17.
Harmonic Spectrum of Output Voltage of Lagging Load (R=10 Ω, L=15 mH) at $m_a = 1.0$

5.2. Efficiency Analysis

The efficiency of the proposed MLI is measured experimentally in this section when the frequency of the PDPWM carriers is 4 kHz. The measurement results are listed in Table 4. Although, both simulation and experiemental measurements are close to each other, it is found generally that the efficiency of the proposed MLI in the experiments is lower than that of the simulation studies. More specifically, when the modulation index $m_a = 1.0$, the efficiency is measured as 94.38 % for resistive load in the experiments, while the efficiency is 95.73 % in the simulation study for the same load type. Similarly, the efficieny of the proposed MLI under lagging load in the experiments and the simulation studies are 94.64 % and 98.74 % respectively. The reason of the differences between the efficiencies of the simulated and the experimentally verified MLI is that the switching and the conduction losses of the MOSFETs were not accounted in the simulation studies. Moreover, the heating of the remaining circuit components was not considered in the simulation studies. Finally, it can be concluded that these differences are very little and the efficiency measurement results are consistent with each other for all load types.

Table 4.
Efficiency Measurements of the Hardware Prototype of the Proposed MLI at $m_a = 1.0$

	Load type	Input power	Output power	Efficiency
Simulation results	Resistive ($R = 10\ \Omega$)	65.98 W	63.17 W	95.74 %
	Inductive (R= $10\ \Omega, L = 15\ mH$)	52.45 W	51.79 W	98.74 %
Experimental results	Resistive $R = 10\ \Omega$	60.50 W	57.10 W	94.38 %
	Inductive (R= $10\ \Omega, L = 15\ mH$)	37.30 W	35.30 W	94.64 %

6. Conclusion

The researchers continuously highlight the importance of energy saving and increasing power quality in power electronic systems. One way to increase the power quality of the inverters is to increase the level number at the output. But this situation at the same time increases inverter losses due to the increasing number of switching elements. Since more semiconductors are needed in order to obtain more levels at the output. Using more semiconductors also increases the failure rates that worsens system reliability. In this study, a single-phase asymmetric hybrid multi-level inverter is proposed, designed, and experimentally verified. The power circuit of the proposed multi-level inverter is built by combining a neural point clamped module and an H-bridge module. For asymmetrical operation, two different DC sources with different magnitudes are used as inputs to increase the level number at the output without increasing the number of semiconductors. The switching pulses for the MOSFETs are generated according to phase disposition pulse width modulation algorithm. The proposed multi-level inverter has a

flexible characteristics by varying the modulation index and can generate a maximum of seven-levels at the output voltage when the modulation index is set to one. The harmonic performance and the efficieny of the proposed multi-level inverter are inspected in both simulation and experimental environment under different power factor loads. There are some differences observed between simulation and experimental measurements, which are also commented. It is experiementally verified that the proposed multi-level inverter has a maximum efficiency of 94 %, while the total harmonic distortion at the output voltage is found as around 29 %.

References

Abraham B. T. and Benny A. (2014). "NPC-H bridge multilevel inverter using third harmonic injection," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 3, pp. 174-181.

Akagi H. (2017). "Multilevel converters: Fundamental circuits and systems," Proceedings of the IEEE, vol. 105, pp. 2048-2065.

Arslan A. O., Eroğlu F., Kurtoğlu M. and Vural A. M. (2019. "Optimal carrier frequency swapping for PD-PWM in modular multilevel converter," ISMSIT '19 Proceedings of the 3rd International Symposium on Multidisciplinary Studies and Innovative Technologies, pp. 1-6.

Barnes M., Van Hertem D., Teeuwsen S. P. and Callavik M. (2017). "HVDC systems in smart grids," Proceedings of the IEEE, vol. 105, pp. 2082-2098.

Buccella C., Cimoroni M. Tinari G., M. and Cecati C. (2019). "Seven-level cascaded inverters for uninterruptible power supply (UPS) applications," IECON '19 Proceedings of the 45th Annual Conference of the IEEE Industrial Electronics Society, pp. 1549-1554.

Chattopadhyay S. K., Chakraborty C. and Pal B. C. (2012). "Cascaded h-bridge & neutral point clamped hybrid asymmetric multilevel inverter topology for grid interactive transformerless photovoltaic power plant," IECON '12 Proceedings of the 38th Annual Conference on IEEE Industrial Electronics Society, pp. 5074-5079.

Chen H. C., Wu P. H., Lee C. T., Wang C. W., Yang C. H. and Cheng P. T. (2016). "A flexible DC voltage balancing control based on the power flow management for star-connected H-bridge converter," IEEE Transactions on Industrial Applications, vol. 52, pp. 4946-4954.

Corzine K. and Familiant Y. (2002). "A new cascaded multilevel H-bridge drive," IEEE Transactions on Power Electronics, vol. 17, pp. 125-131.

El-Zohri E. H. and Mosbah M. A. (2019). "Comparative evaluation of PWM techniques used at mega 328/p with PI control for inverter-fed induction motor," ITCE '19 Proceedings of the International Conference on Innovative Trends in Computer Engineering, pp. 219-224.

Giri S. K., Banerjee S. and Chakraborty C. (2019). "An improved modulation strategy for fast capacitor voltage balancing of three-level NPC inverters," IEEE Transactions on Industrial Electronics, vol. 66, pp. 7498-7509.

Hasan N. S., Rosmin N., Osman D. A. A. and Musta'amal Jamal A. H. (2017). "Reviews on multilevel converter and modulation techniques," Renewable and Sustainable Energy Reviews, vol. 80, pp. 163-174.

Holmes D. G. and McGrath B. P. (2001). "Opportunities for harmonic cancellation with carrier-based PWM for two-level and multilevel cascaded inverters," IEEE Transactions on Industrial Applications, vol. 37, pp. 574-582.

Islam M. R., Guo Y. and Zhu J. (2013). "A high-frequency link multilevel cascaded medium

voltage converter for direct grid integration of renewable energy systems," IEEE Transactions on Power Electronics, vol. 29, pp. 4167-4182.

Karasani R. R., Borghate V. B., Meshram P. M., Suryawanshi H. M. and Sabyasachi S. (2017). "A three-phase hybrid cascaded modular multilevel inverter for renewable energy environment," IEEE Transactions on Power Electronics, vol. 32, pp. 1070-1087.

Kumar P. R., Kaarthik R. S., Gopakumar K., Leon J. I. and Franquelo L. G. (2015). "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges," IEEE Transactions on Power Electronics, vol. 30, pp. 3471-3478.

Li Z., Khajepour A. and Song J. (2019). "A comprehensive review of the key technologies for pure electric vehicles," Energy vol. 182, pp. 824-839.

Ma Y., Hong F., Zhou X. and Gao Z. (2018). "An overview on harmonic suppression," CCDC '18 Proceedings of the Chinese Control and Decision Conference, pp. 4943-4948.

Mali R., Adam N., Satpaise A. and Vaidya A. P. (2019). "Performance comparison of two level inverter with classical multilevel inverter topologies," ICECCT '19 Proceedings of the IEEE International Conference on Electrical, Computer and Communication Technologies, pp. 1-7.

Montesinos-Miracle D., Massot-Campos M., Bergas-Jan J., Galceran-Arellano S. and Rufer A. (2013). "Design and control of a modular multilevel DC / DC converter for regenerative applications," IEEE Transactions on Power Electronics, vol. 28, pp. 3970-3979.

Narmatha R., and Govindaraj T. (2013). "Inverter dead-time elimination for reducing harmonic distortion and improving power quality," International journal of Asian Scientific Research, vol. 3, pp. 247-257.

Peng F.Z., Qian W. and Cao D. (2010). "Recent advances in multilevel converter/inverter topologies and applications," IPEC '10 Proceedings of the International Power Electronics Conference -Asia, pp. 492-501.

Rashid M. H. (2001). "Power Electronics Handbook," Academic Press Series in Engineering, London, pp. 211-224.

Rivera S., Kouro S., Wu B., Leon J. I., Rodriguez J. and Franquelo L. G. (2011). "Cascaded h-bridge multilevel converter multistring topology for large scale photovoltaic systems," Proceedings of the IEEE International Symposium on Industrial Electronics, pp. 1837-1844.

Sahoo A. K., Mahmud K., Crittenden M., Ravishankar Padmanaban J., S. and Blaabjerg F. (2020). "Communication-less primary and secondary control in inverter-interfaced AC microgrid: An overview," IEEE Journal of Emerging and Selected Topics in Power Electronics.

Shults T. E., Filatova A. S., Dybko M. A. and Husev O. O. (2018). "SVPWM capacitor balancing method for single-phase three-level NPC impedance-source inverters," EDM '18 Proceedings of the 19th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices, pp. 6403-6407.

Vijeh M., Rezanejad M., Samadaei E. and Bertilsson K. (2019). "A review of multilevel based on main submodules: Structural point of view," IEEE Transactions on Power Electronics, vol. 34, pp. 9479-9502.

Viju Nair R., Chattopadhyay R., Parashar S., Bhattacharya S. and Gopakumar K. (2018). "Cascaded active neutral point clamped and flying capacitor inverter topology for induction motor drives applications," ECCE '18 Proceedings of the IEEE Energy Conversion Congress and Exposition, pp. 6696-6702.

Xiaofang S., Binbin R., Yongsheng Z. (2011). "Optimal dead-time elimination for voltage source inverters," In: Ma M. (eds) Communication Systems and Information Technology, vol 100 of Lecture Notes in Electrical Engineering, pp. 617-624, Springer, Berlin, Heidelberg.

Zeb K., Uddin W., Khan M. A., Ali Z., Ali M. U., Christofides N. and Kim H. J. (2018). "A comprehensive review on inverter topologies and control strategies for grid connected photovoltaic system," Renewable and Sustainable Energy Reviews, vol. 94, pp. 1120-1141.

Zheng Z., Wang K., Xu L. and Li Y. (2013). "A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles," IEEE Transactions on Power Electronics, vol. 29, pp. 3537-3546.